## AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the present application.

**Listing of Claims:**

**Claim 1 (currently amended):** A wafer holder for semiconductor manufacturing equipment, the wafer holder having a surface for carrying wafers and comprising a layer of electrical circuitry composed of one or more sinter laminae, formed either on the face or in the interior of the wafer holder, said circuit layer being as its main constituent one or more metals selected from tungsten, molybdenum and tantalum and having porosity in that pores are present therein, said porosity being in the range from 0.1% to 40%.

**Claims 2 and 3 (canceled)**

**Claim 4 (currently amended):** A wafer holder as set forth in claim [[2]] 1, wherein said electrical circuitry any of an electrode circuit for an electrostatic chuck, a resistive-heating-element circuit, an RF-power electrode circuit, and a high-voltage-generating electrode circuit.

**Claim 5 (currently amended):** A wafer holder as set forth in claim [[3]] 19, wherein said electrical circuitry is any of an electrode circuit for an electrostatic chuck, a resistive-heating-element circuit, an RF-power electrode circuit, and a high-voltage-generating electrode circuit.

**Claim 6 (original):** Semiconductor manufacturing equipment wherein the wafer holder set forth in claim 1 is installed.

**Claim 7 (canceled)**

**Claim 8 (currently amended):** Semiconductor manufacturing equipment wherein the wafer holder set forth in claim [[3]] 19 is installed.

**Claim 9 (original):** Semiconductor manufacturing equipment wherein the wafer holder set forth in claim 4 is installed.

**Claim 10 (original):** Semiconductor manufacturing equipment wherein the wafer holder set forth in claim 5 is installed.

**Claim 11 (previously presented):** The wafer holder of claim 1, wherein the porosity is in the range from about 0.1 to about 5 percent.

**Claim 12 (currently amended):** The wafer holder of claim 1, wherein~~:~~

~~the sinter laminae comprise as its main constituent one or more metals selected from tungsten, molybdenum, and tantalum; and~~

the porosity is in the range from about 0.1 to about 2 percent.

**Claim 13 (previously presented):** The wafer holder of claim 1, wherein:

the sinter laminae comprise as its main constituent one or more metals selected from vanadium and platinum; and

the porosity is in the range from about 2 to about 5 percent.

**Claim 14 (previously presented):** The wafer holder of claim 1, wherein the pores have an average diameter less than the thickness of the sinter laminae, the pores being distributed throughout the thickness of the sinter laminae.

**Claim 15 (previously presented):** The wafer holder of claim 1, wherein said electrical circuitry comprises a heating circuit.

**Claim 16 (previously presented):** The wafer holder of claim 1, wherein the sinter laminae comprise a mixture of at least one metal powder and at least one oxide powder.

**Claim 17 (previously presented):** The wafer holder of claim 16, wherein:

the at least one metal powder comprises at least one member of the group consisting of tungsten, molybdenum, tantalum, vanadium, and platinum; and

the at least one oxide powder comprises at least one member of the group consisting of a group IIa oxide, a group IIIa oxide, aluminum oxide, and silicon oxide.

**Claim 18 (previously presented):** A wafer holder for semiconductor manufacturing equipment, the wafer holder comprising:

a wafer-carrying surface; and

an electrical heating circuit formed either on the wafer-carrying surface or in the wafer holder, and including

a porous sinter layer made up of a mixture of at least one metal powder and at least one oxide powder, the sinter layer therein having a porosity in the range of from about 0.1 to about 40 volume percent of the sinter layer.

**Claim 19 (new):** A wafer holder for semiconductor manufacturing equipment, the wafer holder having a surface for carrying wafers and comprising a layer of electrical circuitry composed of one or more sinter laminae, formed either on the face or in the interior of the wafer holder, said circuit layer being as its main constituent one or more metals selected from silver, vanadium and platinum and having porosity in that pores are present therein, said porosity being in the range from 2% to 40%.